REMARKS

In the Office Action the Examiner noted that claims 1-8 are pending in the application. The Examiner allowed claim 8, rejected claims 1-5 and 7 and objected to claim 6. The applicants submitted a response after final on April 22, 2005 without amending the claims. In a June 1, 2005 Advisory Action the Examiner indicated that the rejection with respect to claims 5-6 had been overcome by the response so that claims 5, 6 and 8 were allowed, while claims 1-4 and 7 remain rejected. The Examiner's rejections are traversed below. Reconsideration and allowance of the above-referenced application is respectfully requested.

The Rejection

On pages 2-5 of the Office Action the Examiner rejected claims 1-4 and 7 as anticipated by U.S. Patent 5,565,856 to Takaba et al.

The Present Claimed Invention Patentably Distinguishes Over the Prior Art

In the Advisory Action the Examiner pointed out that at page 6, line 1 of the prior Amendment, the applicants argued "that an abnormality detection signal is output when the logical output of the bus is fixed to the high or low level for a predetermined time which exceeds a threshold value and equates this with the claimed invention (claim 1, lines 3-4) which uses much broader terminology."

Based on the Examiner's comment above, claims 1 and 7 have been amended so that the language of these claims parallels the arguments previously presented and repeated below.

Referring to claim 1, for example, the present claimed invention is directed to an abnormality detection device for detecting an abnormality in a communication bus. A time counter measures the time during which a logical output of the communication bus remains at a first logic level which is a high level or a low level. A comparator compares the time measured by the timer counter with a threshold value and outputs an abnormality detection signal indicating an abnormality in the communication bus when the time surpasses the threshold value. The abnormality detection device is independent of a CPU controlling the communication bus.

In the rejection the Examiner asserts that the claimed "timer counter to measure a time during which a signal transmitted through said communication bus continues to be a first logic level" is taught by step 825 in Figure 9, time lapse measuring device 945 in Figure 24 and columns 7 and

8, lines 64-67 and 1-24 of Takaba et al.

The timer reset step 825 in Figure 9 measures the time it takes for data transmitted to a communication IC 140 (Figure 1A) to be transferred to a bus 400 via a driver/receiver 145 as described at column 7, lines 51-53. The ABSY signal is set to a high level in a state where the data is input to the communication IC 140, and the ABSY signal is set to a low level in a state where no data is input to the communication IC 140 as described at column 8, lines 25-30 and columns 6, lines 4-16. An abnormality is detected if the data remains in the communication IC 140 after a predetermined time.

As explained in the Amendment filed April 22, 2005, in contrast to Takaba et al., in the present invention, an abnormality detection signal is output when the logical output of the bus remains at the high or the low level for a predetermined time which exceeds a threshold value. This is completely different from the timer of Takaba et al. which measures the time it takes for data transmitted to communication IC 140 to be transferred to the bus 400. Thus, it is submitted that Takaba clearly does not teach or suggest the claimed timer counter which measures "a time during which a logical output of said communication bus remains at a first logic level which is a high level or low level.

In the current Office Action the Examiner appears to take the position that the above-identified features are taught at column 6, lines 3-16 of Takaba et al. This portion of Takaba et al. references Figure 9 which is a flow chart illustrating data transmission and reception between a controller 100 and a diagnosis unit 300. This portion of the specification states that a bus abnormality is determined for bus 400 when bus 400 is not in an idle state for more than a prescribed period of time. It is explained that a timer detects whether the bus is at a low level for more than a predetermined period of time.

After reviewing the above-identified portion of Takaba et al. cited by the Examiner in the "Response to Arguments" section, applicants believe that the cited portion of column 6 is consistent with applicant's prior argument that Takaba et al. measures the time it takes for data transmitted to communication IC 140 to be transferred to the bus 400. In particular, the signal ABSY is found in communication IC 140 and CPU 110 as illustrated in Figure 1B. Therefore, it is submitted that Takaba et al. clearly does not teach or suggest the claimed timer counter which measures "a time during which a logical output of said communication bus remains at a first logic level which is a high level or a low level" as set forth in claim 1.

The Examiner also asserts that the feature wherein the abnormality detection device is independent of the CPU controlling the communication bus, is taught by diagnosis unit 300 in Figure

1A of Takaba et al. In Figure 1A of Takaba et al., the diagnosis unit 300 and the CPU 110 are connected via the bus 400 since the CPU 110 is provided within the controller 100 that is connected to the diagnosis 300 via the bus 400. Further, the diagnosis unit 300 does not appear to be related to the abnormality detection device.

It is clear from Figure 24 and the portions of columns 7 and 8 referenced by the Examiner that the communication abnormality determining step 840 (Figure 9) and the time lapse measuring device 945 (Figure 24) are included in the CPU 110 and not in the diagnosis unit 300. As a result, the Examiner's assertion that the diagnosis unit 300 of Takaba et al. corresponds to the abnormality detection device of the present invention and that the diagnosis unit 300 is independent of the CPU 110 controlling the communication bus 400, is inaccurate.

Column 3, lines 26-32 of Takaba describe that "diagnosis unit 300 can be connected, when diagnosis is necessary, through bus 400 to controllers 100 and 200 thus permitting read out of, for example, abnormality detection data processed by the controllers 100 and 200." Thus, Takaba et al. makes the abnormality detection by the controllers 100 and 200 and not by the diagnosis unit 300. As a result, in view of the above, it is submitted that Takaba et al. fails to teach or suggest the claimed feature "wherein the abnormality detection device is independent of a CPU controlling the communication bus."

In the "Response to Arguments" section of the current Office Action the Examiner responds to the above argument by simply pointing to Figure 1A and item 300 of Takaba et al. However, the Examiner's reference to item 300 is irrelevant because the diagnosis unit 300 does not perform the error detection described with respect to Figure 9 at column 6, lines 3-16. It is clear from this portion of Takaba et al. that the communication abnormality determining step 840 in Figure 9 is performed in the CPU 110 which is a part of the controller 100 for controlling the communication bus. Therefore, applicant maintains the position that Takaba et al. fails to teach or suggest the claimed feature "wherein the abnormality detection device is independent of a CPU controlling the communication bus."

In summary, it is submitted that the prior art does not teach or suggest the claimed abnormality detection device of claim 1 which includes:

> a timer counter to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level; and

...wherein the abnormality detection device is independent of a CPU controlling the communication bus.

Therefore, it is submitted that claim 1 patentably distinguishes over the prior art.

Referring to claim 7, it is submitted that the prior art does not teach the claimed microcomputer which includes:

a timer counter to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level; and

...wherein the microcomputer is independent of a CPU controlling the communication bus.

Therefore, it is submitted that claim 7 patentably distinguishes over the prior art.

Claims 2-4, depend, directly or indirectly, from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is submitted that claims 2-4 patentably distinguish over the prior art.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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